AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system for channel coding data within a digital communications system comprising:

a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length; and

an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced, said encoder operative according to the constraint length, and wherein the topology of the trellis corresponds to memory length *m*, and the known symbols are inserted after each *m* symbols within the input data sequence.

2. (Original) A system according to Claim 1, wherein the known symbols that are inserted comprise zeros.

3. (Canceled)

4. (Original) A system according to Claim 1, wherein said encoder comprises a convolutional encoder

5. (Original) A system according to Claim 1, wherein the encoder applies code words that are one-to-one mappings of the distinct paths on a trellis to binary sequences.

6. (Canceled)

7. (Original) ~~A system according to Claim 1,~~ A system for channel coding data within a digital communications system comprising:

a data receiving circuit for receiving a digital input data sequence and periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length; and

an encoder operatively connected to said data receiving circuit for trellis encoding the expanded digital input data sequence to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced, said encoder operative according to the constraint length, wherein the encoder is operative as a generator matrix having a constraint length k=m-1, wherein m corresponds to the memory length, and the code rate is R=1/1 such that the known symbols are inserted after each k-1 information bit.

8. (Original) A system according to Claim 1, and further comprising a Maximum Likelihood (ML) decoder for receiving and decoding the channel coded data stream.

9. (Original) A system according to Claim 8, wherein the Maximum Likelihood (ML) decoder comprises a Viterbi decoder.

10. (Currently Amended) A method of channel coding data in a digital communications system comprising the steps of :

receiving a digital input data sequence;

periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length; and

trellis encoding the expanded digital input data sequence based on the constraint length to produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced, wherein the topology of the trellis corresponds to the memory length *m*, and further comprising the step of inserting a known symbol after each *m* symbols within the input data sequence.

11. (Original) A method according to Claim 10, wherein the step of inserting known symbols comprises the step of inserting zeros into the digital input data sequence.

12. (Canceled)

13. (Original) A method according to Claim 10, and further comprising the step of applying code words that are one-to-one mappings of the distinct paths on a trellis to binary sequences.

14. (Canceled)

15. (Original) A method according to Claim 10, and further comprising the step of decoding channel coded data stream within a maximum likelihood (ML) decoder.

16. (Original) A method according to Claim 15, and further comprising the step of decoding the channel coded data stream within a Viterbi decoder.

17. (Previously Presented) A method of channel coding data in a digital communications system comprising the steps of:

receiving a digital input data sequence;

periodically inserting known symbols into the digital input data sequence and forming an expanded digital input data sequence based on a constraint length k=m-l, wherein m corresponds to a memory length and a code rate is R=1/l, such that the known symbols are inserted after each k-l information bit; and

trellis encoding the expanded digital input data sequence to produce a channel coded data stream, wherein the number of connections between trellis nodes in a trellis are reduced.

18. (Original) A method according to Claim 17, wherein the step of inserting known symbols comprises the step of inserting zeros into the digital input data sequence.

19. (Canceled)

20. (Original) A method according to Claim 17, and further comprising the step of applying code words that are one-to-one mappings of the distinct paths on a trellis to binary sequences.

21. (Original) A method according to Claim 17, and further comprising the step of decoding channel coded data stream within a maximum likelihood (ML) decoder.

22. (Original) A method according to Claim 21, and further comprising the step of decoding the channel coded data stream within a Viterbi decoder.